

JUN 13 2003

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Sheet 1 of 1

U.S. Department of Commerce, Patent and Trademark Office	Atty. Docket No.	Serial No.				
	M-15327 US	10/772,932				
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Applicant(s)				
(Use several sheets if necessary)		Chia-Shun Hsiao et al.				
	Filing Date	Group				
	Feb. 4, 2004	2818				
U.S. Patent Documents						
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
<i>CHL</i>	6,403,417	06-2002	Chien et al.			—
<i>CHL</i>	6,451,708	09-2002	Ha			—
<i>J</i>						
<i>D</i>						
<i>E</i>						
<i>F</i>						
<i>G</i>						
<i>H</i>						
<i>I</i>						
<i>J</i>						
<i>K</i>						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)						
<i>CHL</i>	L	Naruke, K.; Yamada, S.; Obi, E.; Taguchi, S.; and Wada, M. "A New Flash-Erase EEPROM Cell with A Sidewall Select-Gate On Its Source Side," 1989 IEEE, pp. 604-606.				
<i>CHL</i>	M	Hu, A.T.; Chan T.Y.; Ko, P.K.; and Hu, C. "A Novel High-Speed, 5-Volt Programming EPROM Structure With Source-Side Injection," 1986 IEEE, 584-587.				
<i>CHL</i>	N	Kizutani, Yoshihisa; and Makita, Koji "A New EPROM Cell With A Sidewall Floating Gate For High-Density and High Performance Device," 1985 IEEE, 635-638.				
<i>CHL</i>	O	Ma, Y.; Pang, C.S.; Pathak, J.; Tsao, S.C.; Chang, C.F.; Yamauchi, Y.; Yoshimi, M. "A Novel High-Density Contactless Flash Memory Array Using Split-Gate Source-Side-Injection Cell for 5V-Only Applications," 1994 Symposium on VLSI Technology Digest of Technical Papers, pp. 49-50.				
<i>CHL</i>	P	Mih, Rebecca et al. "0.18um Modular Triple Self-Aligned Embedded Split-Gate Flash Memory," 2000 Symposium on VLSI Technology Digest of Technical Papers, pp. 120-121.				
Examiner	<i>CHL</i>	Date Considered	<i>7/25/05</i>			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.						

U.S. Department of INFORM TIO	U.S. Patent and Trademark Office		Atty. Docket No.	Serial No.		
			M-15327 US	Unassigned		
CLOSURE STATEMENT BY APPLICANT (several sheets if necessary)		Applicant(s) Chia-Shun Hsiao et al.				
		Filing Date	Group			
		Herewith	Unassigned			
U.S. Patent Documents						
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
CHC	03/0067806	10 Apr. 2003	Tuan	—	—	—
CHC	055,524	12 Mar. 2002	Tuan et al.	—	—	—
CHC	541,324	1 Apr. 2003	Wang	—	—	—
AD						
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)						
Naruke et al., "A New Flash-Erase EEPROM Cell with a Sidewall Select-Gate on Its Source Side", M Technical Digest 1989, pages 603-606.						
United States Application No.: 10/402,698 filed March 28, 2003 by Chung et al.						
Chih et al., "0.18um Modular Triple Self-Aligned Embedded Split-Gate Flash Memory", 2000 Symposium on VLSI Technology, Digest of Technical Papers, pages 120-121.						
Examiner	Date Considered	7/25/05				
Indicate considered, whether or not citation is in conformance with MPEP 609; Draw line through and not considered. Include copy of this form with your communication to applicant.						